## IN THE CLAIMS

1.(Amended) A transistor comprising:

a source region, a drain region, and a channel region between the source and drain regions in a semiconductor surface layer formed on an underlying insulating portion, and an electrically interconnected gate formed of a silicon carbide material.

6.(Amended) The transistor of claim 1, wherein the silicon carbide gate material is described by $Si_{1-X}C_X$ and X is approximately less than or equal to 0.5.

15.(Amended) A semiconductor memory device comprising:

a memory array including a plurality of transistors, at least one of the transistors in a semiconductor surface layer formed on an underlying insulating portion and including an electrically interconnected gate formed of a silicon carbide material;

addressing circuitry for addressing the memory array; and

control circuitry for controlling read, write, and erase operations of the memory device.

Please add the following new claims:

22.(New) The integrated circuit device of claim 11 wherein the substrate comprises a semiconductor surface layer formed on an underlying insulating portion.

23.(New) The semiconductor memory device of claim 11 wherein each silicon carbide gate comprises $Si_{1-X}C_X$ and X is approximately less than or equal to 0.5.

24.(New) The semiconductor memory device of claim 15 wherein each of the transistors in the memory array comprises:

a source region, a drain region, and a channel region between the source and drain regions in a semiconductor surface layer formed on an underlying insulating portion; and

an electrically interconnected gate formed of a silicon carbide material.

25.(New) The semiconductor memory device of claim 15 wherein pairs of the transistors in the memory array comprise:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and separated therefrom by an insulating layer; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and separated therefrom by an insulating layer.

26.(New) The semiconductor memory device of claim 25 wherein the substrate comprises a semiconductor surface layer formed on an underlying insulating portion.

27.(New) The semiconductor memory device of claim 15 wherein the silicon carbide gate comprises polycrystalline silicon carbide.

28.(New) The semiconductor memory device of claim 15 wherein the silicon carbide gate comprises microcrystalline silicon carbide.

29.(New) The semiconductor memory device of claim 15 wherein the silicon carbide gate is separated from the semiconductor surface layer by an insulating layer of silicon oxide.

30.(New) The semiconductor memory device of claim 15 wherein the silicon carbide gate comprises $Si_{1-X}C_X$ and X is approximately less than or equal to 0.5.

31.(New) A semiconductor memory device comprising:

a memory array including a plurality of transistors wherein pairs of the transistors comprise:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and separated therefrom by an insulating layer; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and separated therefrom by an insulating layer;

addressing circuitry for addressing the memory array; and

control circuitry for controlling read, write, and erase operations of the memory device.

32.(New) The semiconductor memory device of claim 31 wherein the substrate comprises a semiconductor surface layer formed on an underlying insulating portion.

33.(New) The semiconductor memory device of claim 31 wherein each silicon carbide gate comprises polycrystalline silicon carbide.

34.(New) The semiconductor memory device of claim 31 wherein each silicon carbide gate comprises microcrystalline silicon carbide.

35.(New) The semiconductor memory device of claim 31 wherein each an insulating layer comprises silicon oxide.

36.(New) The semiconductor memory device of claim 31 wherein each silicon carbide gate comprises $Si_{1-X}C_X$ and X is approximately less than or equal to 0.5.